In the specification:

Please substitute the following paragraphs for the paragraphs at the indicated locations in the specification as originally filed.

Page 9, line 33+:

The transistors 20 and 21 are otherwise of similar construction; each having a gate dielectric 205, 215, a gate electrode 208, 218, a sidewall spacer structure ~~12~~ ~~10~~ and source, drain and gate silicide regions 19 as will be familiar to those skilled in the art and which are preferably formed by an implant self-aligned to sidewall spacers ~~11~~ 10. Extension and halo implants, graded junctions and the like may also be provided.

Page 10, line 21+:

Fig. 2 shows the first step taken in forming the invention shown in Fig. 6 from the basic structure shown in Fig. 1. This step includes the deposit of a stressed film 11 (e.g. tensile) over the remaining structure of Fig. 1 in order to produce stress (e.g. tensile) in the channels 201, ~~218~~ 211 of the transistors 20 and 21. Prior to the deposit of this film, the sidewall spacers 11 are optionally removed. The highly stressed film is preferably silicon nitride (Si_3N_4) or silicon oxynitride ($Si_3O_xN_y$) or a combination of both. These materials can be deposited in a highly stressed form providing either tensile or compressional stress, depending on particular process parameters such as plasma power and gas flow rates. For example, using a PECVD process, the stress level is mainly controlled by plasma power and, in general, yields a compressive stress. Thermal CVD Si_3N_4 is deposited at a temperature above 600°C and is normally tensile. Application of this tensile stress enhances the performance of the nMOS transistor 20 while decreasing the performance abilities of the pMOS transistor 21.

Page 11, line 10+:

Fig. 3 illustrates the second step taken toward reaching the exemplary final configuration shown in Fig. 6. In this step, a dielectric 12 (e.g. oxide) is deposited onto the structure shown in Fig. 2 via high density plasma deposition (HDP) and, for example, chemical-mechanical polish, CMP stopping on nitride 11 and then etched back to oxide 12 to form the illustrated configuration. The thickness of the oxide layer 12 is not critical to the practice of the invention, although layer thickness is preferably in the range of 50-100 nm. The dielectric 12 is preferably a non-stressed oxide or other non-stressed material to serve as an etch stop for the etch back and a neutral barrier to shear forces and stresses between the tensile film 11 and the later applied compressive film 13.

Page 12, line 2+:

Fig. 5 illustrates the fourth step taken toward reaching the exemplary final configuration shown in Fig. 6. The existing dielectric material 12 (shown in Fig. 4) is removed and a new dielectric layer 120 is deposited over both gate electrodes 208, 218 as shown over the nMOS transistor 20. This layer 120 serves to isolate stresses from later-applied layers (e.g. in shear) from reaching the substrate. A blockout photo-resist 22 is applied and the dielectric and stressed film are largely removed around the pMOS transistor 21 by etching. As a result of this step, the nMOS transistor 20 is still influenced by the tensile film 11 and still maintains an enhanced level of performance, while the pMOS transistor 21 is no longer suffering a degradation of performance but resumes a normal potential performance as a result of the removal of the tensile stress provided by the stressed film 11.

Page 13, line 3+:

Fig. 7 is a graphical representation of the resulting lateral stress levels applied to the transistors through application of this invention in simulation. This graph is based on the stress level on the transistors at a location 5 nm below the gate dielectrics 205, 215 and a stressed film thickness of 50 nm using stressed nitride for both the tensile film and the compressive film. The resulting stress on the defined areas based on the defined conditions is approximately +190MPa in the nMOS transistor channel 201 and -300MPa in the pMOS transistor channel 211. Thus, it is seen that tensile and compressive stresses are produced substantially ~~coexensive in~~ coextensive with the transistor channels 201, 211 on the same substrate 14.

Page 14, line 23+:

Further, in regard to the pMOS transistor, the preferred embodiment (Fig. 6) includes a dielectric layer 120,17 surrounding the majority of the oxide liner ~~19~~ 15 of the gate electrode 218 with exception to the top of the gate which is left to make contact with the compressive film 13. The second embodiment does not include the aforementioned dielectric layer and therefore, the entirety of the oxide liner 19 surrounding the sides of the gate electrode 218 is in contact with the compressive film 13 which makes direct contact with the top of the gate electrode 218. These differences between the first and second embodiments do not effect the stress levels within the channels 201, 211 and therefore said first and second embodiments, when compared, exhibit no significant difference from one another in potential carrier mobility.